



PATENT
Attorney Docket No.: K35A1302

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
RALPH H. CASTRO et al.

Application No.: 10/627,512

Filed: September 25, 2003

For: RANGE-BASED CACHE CONTROL
SYSTEM AND METHOD

) Group Art Unit: 2187
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OCT 22 2003

DECLARATION OF RALPH H. CASTRO
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Ralph H. Castro, hereby declare as follows:

1. I am a joint inventor in parent application number 09/552,399 (the "Parent Application"), now patent number 6,601,137, and I am a joint inventor in this continuation application number 10/627,512 (the "Continuation Application") which claims priority to the Parent Application. I am making this declaration to establish facts showing that the invention claimed in this Continuation Application was reduced to practice before January 25, 2000, which I am informed is the issue date of U.S. Patent Number 6,018,789 to Sokolov et al. (the "Sokolov '789 patent"). I will hereinafter refer to January 25, 2000 as the "Effective Date" of the Sokolov '789 patent.

In re Application of:
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2. I was employed by the original assignee, Western Digital Corporation ("WDC") at WDC's Irvine facility in the State of California, during the time between my conception of the invention recited in claims 1-6, 9-14 and 17-22, which claims are being pursued in this Continuation Application, and the filing of the Parent Application.

3. I have read claims 1-6, 9-14 and 17-22 and have a technical understanding of how such claims relate to the disclosure of the Parent Application and this Continuation Application.

4. I helped develop and reduce to practice, in the United States of America, a hard disk drive having an integrated circuit to which claims 1-6, 9-14 and 17-22 apply prior to the Effective Date of the Sokolov '789 patent. This particular disk drive was called "Rebel" during its development. The Rebel disk drive, as reduced to practice, included a cache memory and a cache control system that implemented a cache method for servicing host commands. The cache memory had a plurality of memory clusters for caching disk data of disk sectors identified by logical block addresses. The cache control system had a tag memory and a scan engine. The tag memory had a plurality of tag records. Each tag record defined a variable length segment of the memory clusters for caching disk data for a range of logical block addresses and indicated the range of logical block addresses. The scan engine was only usable for scanning the tag records. The scan engine included means for receiving a range of logical block addresses associated with a host command, means for reading the ranges of logical block addresses defined by the tag records, means for comparing the range of logical block addresses associated with the host command with the ranges of logical block addresses indicated in the tag records, and means for providing scan results, based on a comparison by the means for comparing, indicating overlap between the logical block address range associated with the host command and the ranges of logical block addresses indicated in the tag records. The means for comparing further determined whether a first logical block address of a range of logical block addresses associated with a host command was within the ranges of logical block addresses indicated in the tag

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memory records. The means for providing scan results indicated the tag records, determined by the means for comparing, having a range including the first logical block address. The means for providing scan results indicated whether an entire logical block address range, a portion of the logical block address range, or none of the logical block address range associated with a host command is within the ranges of logical block addresses in the tag memory records. The means for providing scan results also indicated whether the logical block address range associated with a host command is within a range of the ranges of logical block addresses in the tag records such that a start logical block address for the host command is greater than a start logical block address for the overlapping tag record range, or whether only a portion of the logical block address range associated with a host command is within a range of the ranges of logical block addresses in the tag memory records. Further, the means for providing scan results indicated whether the portion of the logical block address range associated with a host command that is within a range of the ranges of logical block addresses in the tag records included the beginning or the end of the logical address range associated with the host command.

5. Attached hereto as Exhibit "A" is an assembly tree of a Rebel disk drive. The Rebel disk drive included an ASSEMBLY PCB 61-600840-XXX (see arrow). The assembly tree is dated before the Effective Date of the Sokolov '789 patent (see revision dates in the upper right hand corner).

6. Attached hereto as Exhibit "B" is a Bill of Materials Report for an ASSEMBLY PCB 61-600840-001, which includes an integrated circuit: IC WD70C10SW/I285S (see arrow on page 2).

7. Attached hereto as Exhibit "C" are a Title page (page 1) and a select portion of a Table of Contents (pages 8-10) of a Device Specification for the integrated circuit IC WD70C10SW/I285S. The integrated circuit includes the cache control system (see arrow pointing to heading 10 on page 8) and the tag memory (see arrow pointing to heading 11 on page

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9) that enable the Rebel disk drive to implement the cache method. The Device Specification is dated before the Effective Date of the Sokolov '789 patent.

9. This declaration factually establishes that the claimed invention was reduced to practice in the United States before the Effective Date of the Sokolov '789 patent.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application and any patent issuing thereon.

October
Date: September 13, 2003
Chandler, Arizona
(city)


Ralph H. Castro

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Attorney Docket No.: K35A1302

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Application No.: 10/627,512

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For: RANGE-BASED CACHE CONTROL
SYSTEM AND METHOD

) Group Art Unit: 2187
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) Examiner: Peugh, Brian R.
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OCT 22 2003

DECLARATION OF TSUN Y. NG
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Tsun Y. Ng, hereby declare as follows:

1. I am a joint inventor in parent application number 09/552,399 (the "Parent Application"), now patent number 6,601,137, and I am a joint inventor in this continuation application number 10/627,512 (the "Continuation Application") which claims priority to the Parent Application. I am making this declaration to establish facts showing that the invention claimed in this Continuation Application was reduced to practice before January 25, 2000, which I am informed is the issue date of U.S. Patent Number 6,018,789 to Sokolov et al. (the "Sokolov '789 patent"). I will hereinafter refer to January 25, 2000 as the "Effective Date" of the Sokolov '789 patent.

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5. Attached hereto as Exhibit "A" is an assembly tree of a Rebel disk drive. The Rebel disk drive included an ASSEMBLY PCB 61-600840-XXX (see arrow). The assembly tree is dated before the Effective Date of the Sokolov '789 patent (see revision dates in the upper right hand corner).

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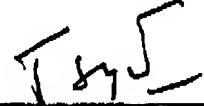
9) that enable the Rebel disk drive to implement the cache method. The Device Specification is dated before the Effective Date of the Sokolov '789 patent.

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10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Application and any patent issuing thereon.

Date: October 15, 2003

ORANGE, California
(city)


Tsun Y. Ng

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In re Application of:
RALPH H. CASTRO et al.

) Group Art Unit: 2187

Application No.: 10/627,512)

) Examiner: Peugh, Brian R.

Filed: September 25, 2003)

RECEIVED
CENTRAL FAX CENTERFor: RANGE-BASED CACHE CONTROL
SYSTEM AND METHOD)

OCT 22 2003

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DECLARATION OF VIRGIL V. WILKINS
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Virgil V. Wilkins, hereby declare as follows:

1. I am a joint inventor in parent application number 09/552,399 (the "Parent Application"), now patent number 6,601,137, and I am a joint inventor in this continuation application number 10/627,512 (the "Continuation Application") which claims priority to the Parent Application. I am making this declaration to establish facts showing that the invention claimed in this Continuation Application was reduced to practice before January 25, 2000, which I am informed is the issue date of U.S. Patent Number 6,018,789 to Sokolov et al. (the "Sokolov '789 patent"). I will hereinafter refer to January 25, 2000 as the "Effective Date" of the Sokolov '789 patent.

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2. I was employed by the original assignee, Western Digital Corporation ("WDC") at WDC's Irvine facility in the State of California, during the time between my conception of the invention recited in claims 1-6, 9-14 and 17-22, which claims are being pursued in this Continuation Application, and the filing of the Parent Application.

3. I have read claims 1-6, 9-14 and 17-22 and have a technical understanding of how such claims relate to the disclosure of the Parent Application and this Continuation Application.

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Date: October 11, 2003

Perris, California
(city)

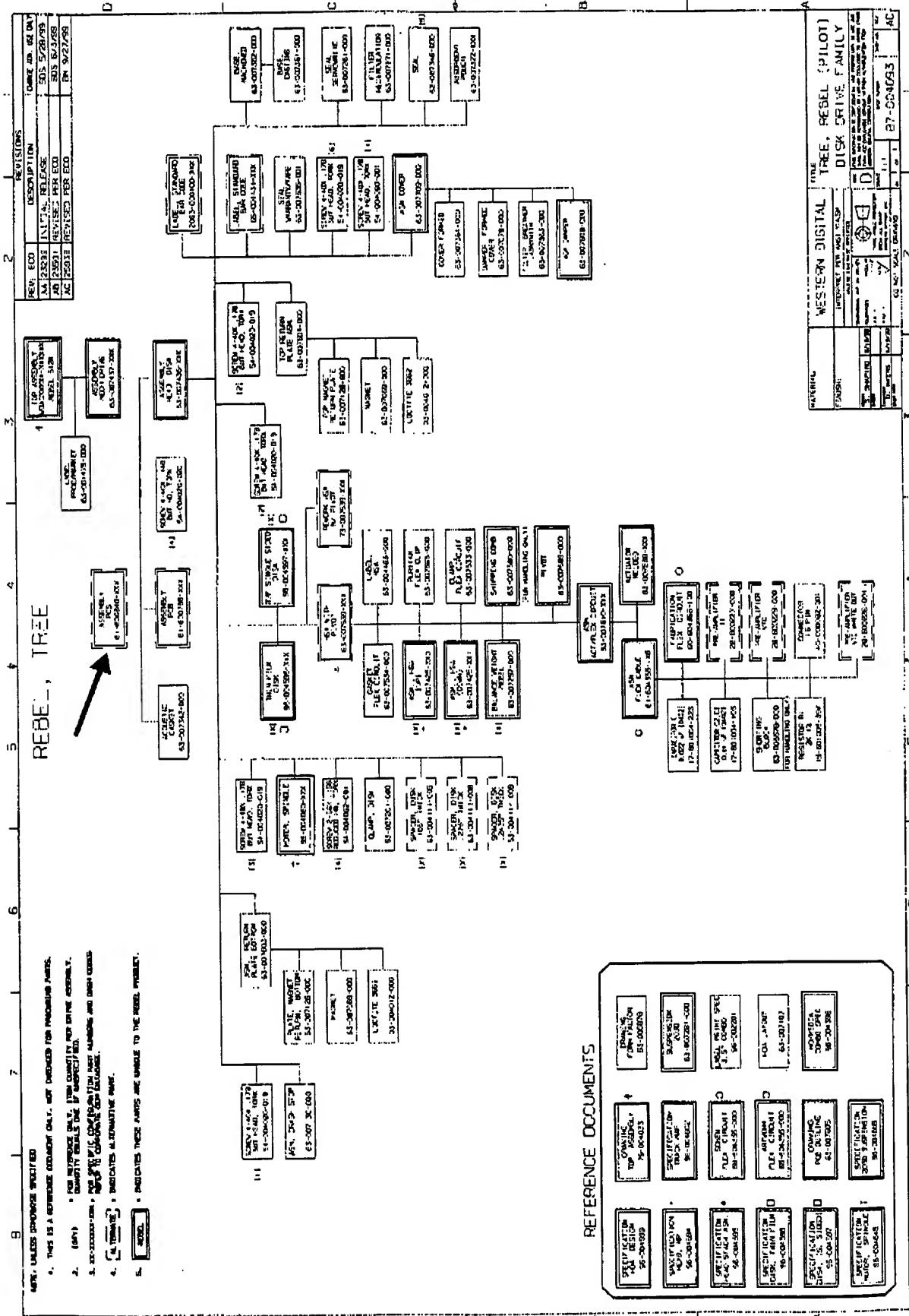


Virgil V. Wilkins

Virgil v. Wilkins

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Exhibit A



REFERENCE DOCUMENTS

Received from <1 760 738 7005> at 10/22/03 4:15:00 PM [Eastern Daylight Time]

BOM Search Results

Exhibit B

Page 1 of 3

WD Bill of Materials Report (Web)

Report Date : Sat, 15 Mar 2003 00:37:33 GMT

Item: 61-600840-001

Rev: E as of 15-MAR-2003 00:37:34 GMT

Org ID:WDC

Desc: PCBA, REBEL ENTEK FLASH

Seq	Item Number	Description	Rev	Qty	Ref Des
1	<u>50-600840-000</u>	PCB ENTEK REBEL / REBEL 2	A	1	
	<u>60-600840-400</u>	PCB, REBEL / REBEL 2 ENTEK 4UP PANEL		1	
	<u>60-600840-X00</u>	PCB, REBEL / REBEL 2 ENTEK CROSSOUT PANEL		1	
3	<u>15-600003-000</u>	RES CM 0.0 OHM 1/10W 0805	A	1	R22
4	<u>15-600004-000</u>	RES CM 0.0 OHM 1/16W 0603	A	4	R34 R38 R41 R57
8	<u>15-600004-345</u>	RES CM 10 OHM 5% 1/16W 0603	A	1	R21
10	<u>15-601004-263</u>	RES CM 80.6 OHM 1% 1/16W 0603	A	2	R12 R13
12	<u>15-600004-357</u>	RES CM 33 OHM 5% 1/16W 0603	A	3	R17 R39 R46
15	<u>15-600004-363</u>	RES CM 56 OHM 5% 1/16W 0603	A	2	R20 R37
17	<u>15-600004-369</u>	RES CM 100 OHM 5% 1/16W 0603	A	7	R23 R29 R3 R30 R35 R4 R40
18	<u>15-600004-376</u>	RES CM 200 OHM 5% 1/16W 0603	A	6	R10 R15 R16 R26 R31 R33
19	<u>15-600004-385</u>	RES CM 470 OHM 5% 1/16W 0603	A	2	R18 R43
20	<u>15-600004-393</u>	RES CM 1.0K 5% 1/16W 0603	A	2	R47 R48
23	<u>15-600004-400</u>	RES CM 2.0K 5% 1/16W 0603	A	3	R49 R50 R51
24	<u>15-600004-417</u>	RES CM 10K 5% 1/16W 0603	A	7	R1 R14 R25 R36 R45 R69 R9
26	<u>15-600004-441</u>	RES CM 100K 5% 1/16W 0603	A	1	R2
29	<u>15-600004-449</u>	RES CM 220K 5% 1/16W 0603	A	2	R5 R70
31	<u>15-600004-489</u>	RES CM 10M 5% 1/16W 0603	A	1	R65
33	<u>15-601001-752</u>	RES CM 1.50 OHM 1% 1/4W 1206	A	2	R67 R68
34	<u>15-601004-301</u>	RES CM 200 OHM 1% 1/16W 0603	A	1	R19
35	<u>15-601004-416</u>	RES CM 3.16K 1% 1/16W 0603	A	1	R64
36	<u>15-601004-423</u>	RES CM 3.74K 1% 1/16W 0603	A	1	R62
37	<u>15-601004-431</u>	RES CM 4.53K 1% 1/16W 0603	A	1	R11
39	<u>15-601004-464</u>	RES CM 10.0K 1% 1/16W 0603	A	1	R55
42	<u>15-601004-560</u>	RES CM 100K 1% 1/16W 0603	A	1	R58
43	<u>15-601004-625</u>	RES CM 475K 1% 1/16W 0603	A	1	R56
45	<u>17-601002-333</u>	CAP CER .033UF 10% X7R 0805	A	1	C49
49	<u>17-600003-101</u>	CAP CER 100PF 5% NPO 50V 0603	A	4	C16 C17 C30

BOM Search Results

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			C51
50	<u>17-600003-150</u>	CAP CER 15PF 5% NPO 50V 0603	A 2 C29 C40
51	<u>17-600003-181</u>	CAP CER 180PF 5% NPO 50V 0603	A 1 C43
52	<u>17-600003-221</u>	CAP CER 220pF 5% NPO 0603	A 1 C63
53	<u>17-600003-391</u>	CAP CER 390pF 5% NPO 25V 0603	A 2 C32 C33
55	<u>17-601003-104</u>	CAP CER 0.1UF 10% X7R 16V 0603	A 1 C62
57	<u>17-601003-332</u>	CAP CER 3300PF 10% X7R 50V 0603	A 10 C11 C15 C19 C21 C27 C28 C34 C39 C4 C6
58	<u>17-601003-154</u>	CAP CER 0.15UF X7R 10% 10V 0603	A 1 C9
59	<u>17-602003-104</u>	CAP CER 0.1UF +80-20% Y5V 25V 0603	A 19 C1 C12 C14 C18 C2 C20 C22 C3 C37 C41 C42 C44 C45 C46 C50 C56 C58 C60 C8
60	<u>17-603006-105</u>	CAP CER 1.0UF X7R 20% 16V 1206	A 2 C31 C35
61	<u>19-600000-194</u>	CAP TANT 10UF 20% 10V (A)	A 1 C57
62	<u>19-600000-193</u>	CAP TANT 4.7UF 20% 10V (A)	A 1 C5
63	<u>19-600000-195</u>	CAP TANT 22uF 20% 10V (B)	A 1 C47
69	<u>19-602000-160</u>	CAP TANT 1.0UF 20% 35V (B)	D 1 C52
70	<u>19-602000-167</u>	CAP TANT 15uF 20% 35V (D)	A 1 C48
72	<u>27-600099-000</u>	IC FLASH 64K*16 35NS 44PLCC	A 1 U2
	<u>43-600065-001</u>	SCKT IC 44PLCC W/O KEY .185H MAX	1
75	<u>27-601123-000</u>	IC SDRAM 1M*16-10 SYNC 50TSOP	A 1 U4
77	<u>28-601018-000</u>	IC LM1117B 3.3V 1.2A 2% REG DPAK	A 1 U6
78	<u>28-601012-000</u>	IC 78M08 8V 2% REG D-PAK	A 1 U7
80	<u>29-600506-000</u>	IC L6262 R2.4 ORCA 44TQFP	A 1 U5
	<u>29-600528-000</u>	IC L6262 R2.6 ORCA 44TQFP	1
82	<u>29-600507-000</u>	IC CLSH3367 R=B2 RIGEL II 100MQFP	A 1 U3
	<u>2029-001003-000</u>	IC CLSH3367 R=B3 RIGEL II DPH 100MQFP	1
	<u>29-600508-000</u>	IC CLSH3367DH-B2 RIGEL-2 100MQFP	1
84	<u>29-601226-000</u>	IC WD70C105W/I285S R=3.0 176TQFP	A 1 U1
86	<u>31-600043-000</u>	DIODE SS14 SHKTY 1A 40V D0214M	B 1 D3
88	<u>32-600051-000</u>	DIODE TVS SMB12A 12V D0214AA	A 1 D2
89	<u>32-600052-000</u>	DIODE TVS SM8J5.0 5V D0214AA	A 1 D1
90	<u>33-600032-000</u>	RESN CER 25MHZ 0.3% 3T 373113	C 1 Y1

3/14/2003

BOM Search Results

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92 <u>39-600091-000</u>	IND FERRITE BEAD POWER 1206	B	5	L1	L2	L3
				L4	L5	
93 <u>41-001321-003</u>	CONN PPHDR 16P2R ST HI-TEMP .045 TAIL	I	1	J1		
94 <u>42-000019-000</u>	CONN Jmpr 2P 6mmX2.54mm CTR WHT	OB	1	J8 (1- 2)		
<u>42-000016-002</u>	CONN Jmpr 2P1R .1CT ST HDL WHT		1			
95 <u>63-006364-000</u>	CONTACT SPRING	B	4	J11	J12	J13
				J14		
96 <u>41-600042-000</u>	CONN CENTURY 54P COMBO SMTMULT	F	1	J2	J3	J8
100 <u>63-001303-000</u>	LABEL BLANK 0.25 X 1.25 INCH	C	1			
101 <u>96-001875</u>	PCBA BARCODE PRINT SPEC.	EA	0			
105 <u>65-600840-000</u>	ARTWORK, REBEL / REBEL 2 ENTEK	A	0			
106 <u>61-600840</u>	PCBA, REBEL ENTEK DWG	A	0			
107 <u>68-600840-000</u>	SCHEMATIC, REBEL ENTEK	B	0			

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Exhibit C

WD70C10 Device Specification

PROJECT LEAD	<i>[Signature]</i>
MGR CONTROLLER DEV	<i>[Signature]</i>

WD70C10
Device Specification

1285s x 3.0

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